Barrys SS-75 Ver 1.3 Motherboard Design

by

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Introduction

Thank you for taking the time in reading this Technological Work. I will be upgrading and adding new features in the Super Sonic 75 Model Design.

This work will use a lot of Visual Designs along with a new file and hashing scheme to promote 8192 block data schemes used for IP frames and packet exchanges . I have combined the SS 65 and 75 model Designs to make improvements on this design itself

I have updated this Motherboard Design to include the following:

1). Four areas of space Private, Public, Shared, and reserved

2). Hashing and Algorithm scheme for second layer OSI Data link layer processing with 8192 Character block data with 8 rows by 1024 Characters matrix with 32frames.

3). 8192 Character Data block tied into the {512 bit address scheme}.

4). 32 layer frame with address entanglement and security

5). Upgraded motherboard to use 4 wires that interface with each other CPU, Memory and video slots

6). CPU utilizes 4 areas of space with total bits 15360 bits and reserved 1024 bits for bit rotting and decay reserved.

7). One memory stick uses 2 banks with total 4 data strings of 128 bits total 512 bits for addressing also memory now has an external reserved area of space.

8). The usage of Data bridges to better process bytes to mac addresses instead of a repeater upgrade from physical to data link layer on the 7 stack OSI layer.

9). Upgraded Hard drive controller from two to three.

10). Introduction to new Cryptographic Model linear and Curvature based Energy

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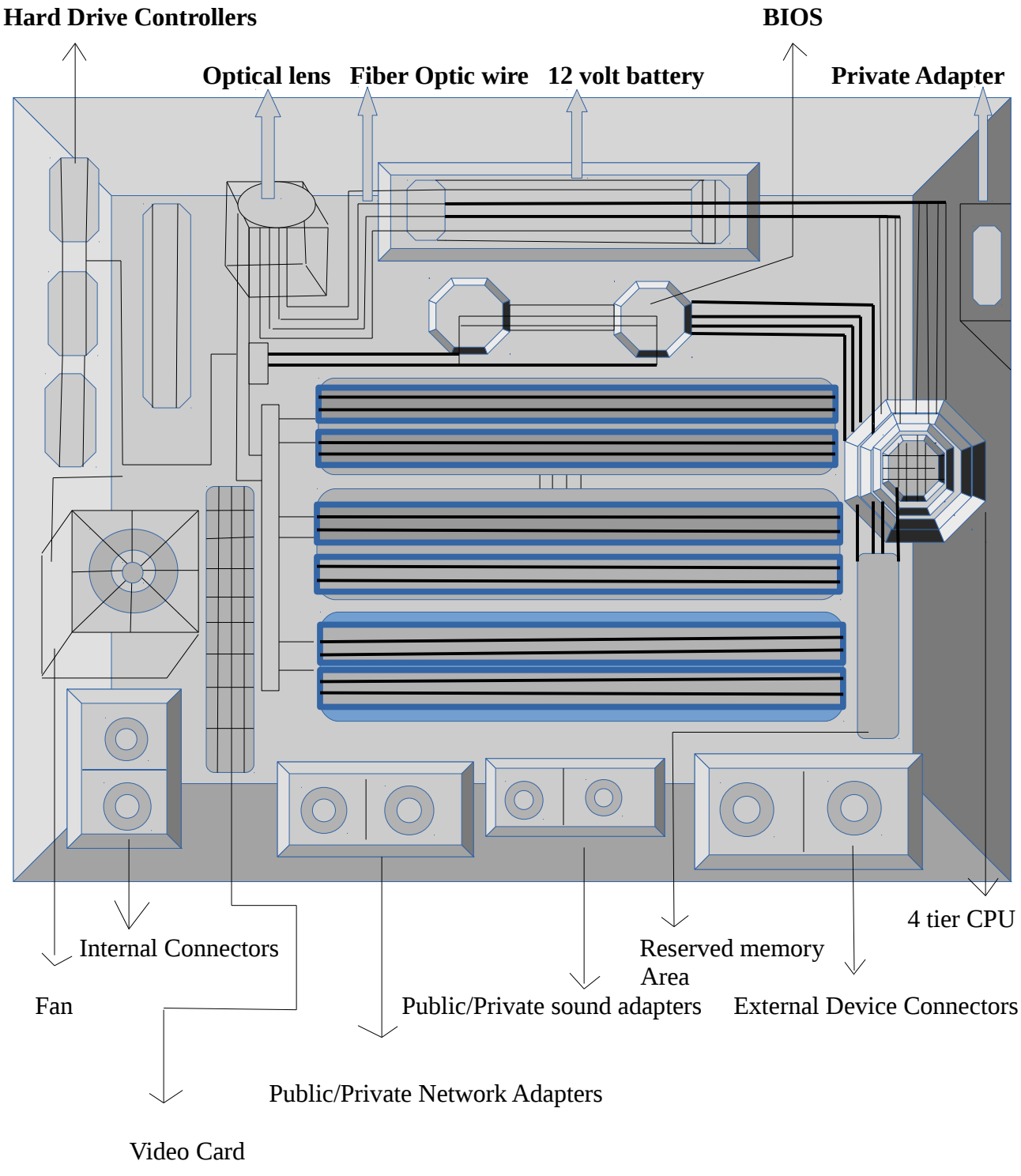
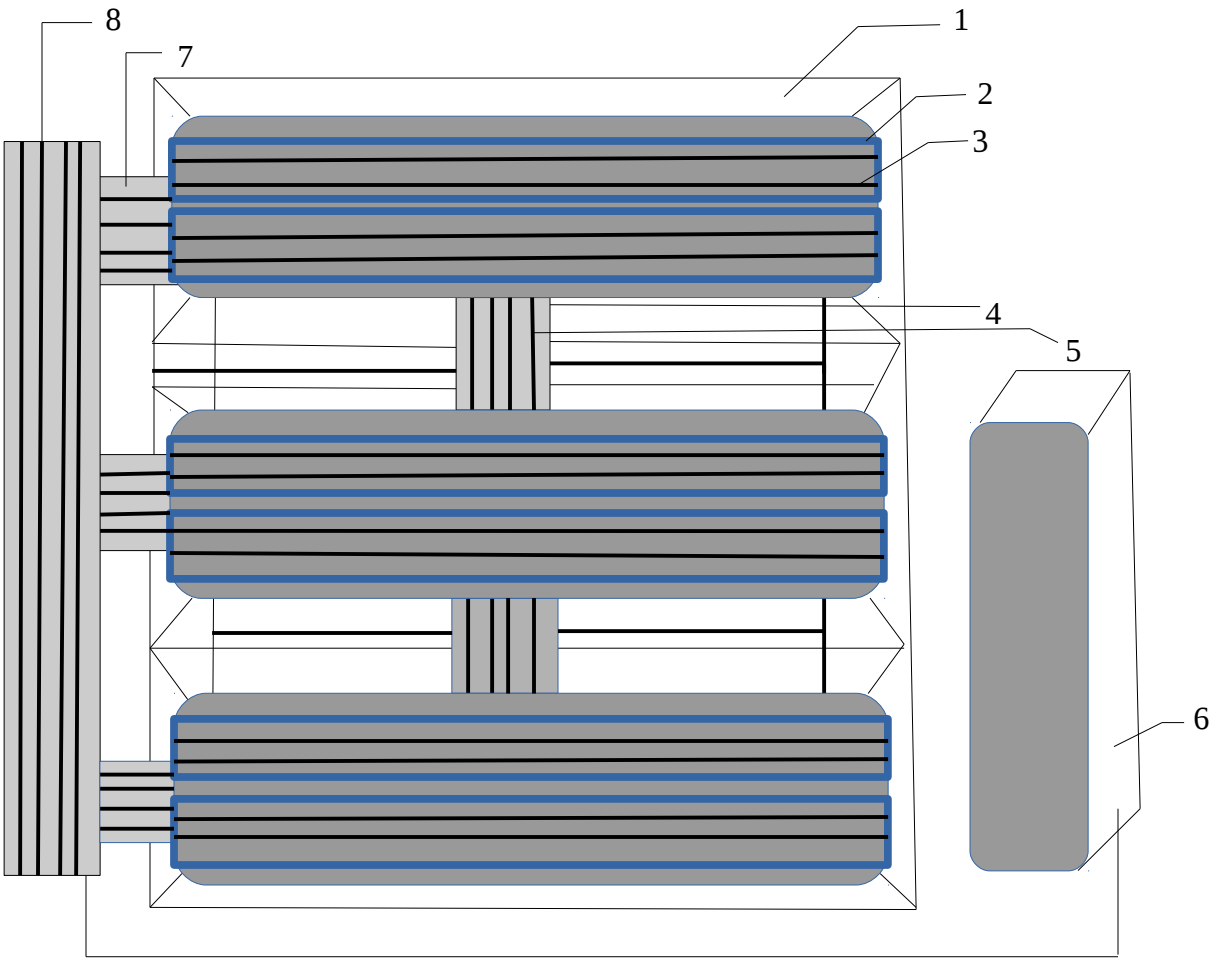
Chapter 1

Visual Design

Model Super Sonic 75 Motherboard- Design Rev 1.3 1-A

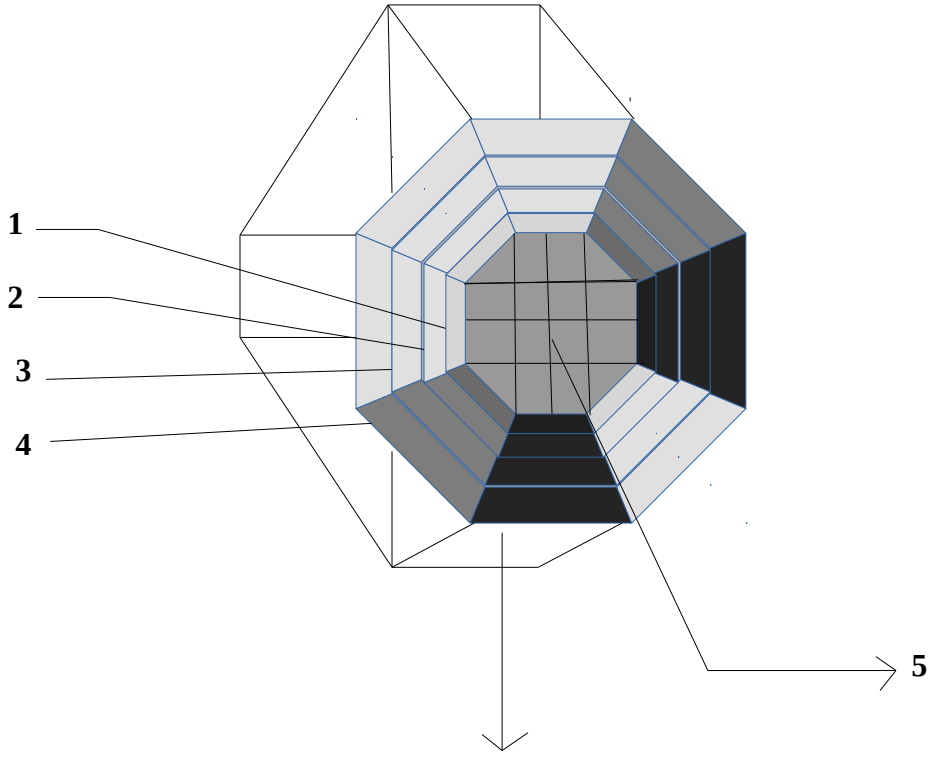


Model Super Sonic 75 Motherboard- Design Rev 1.3 2-A



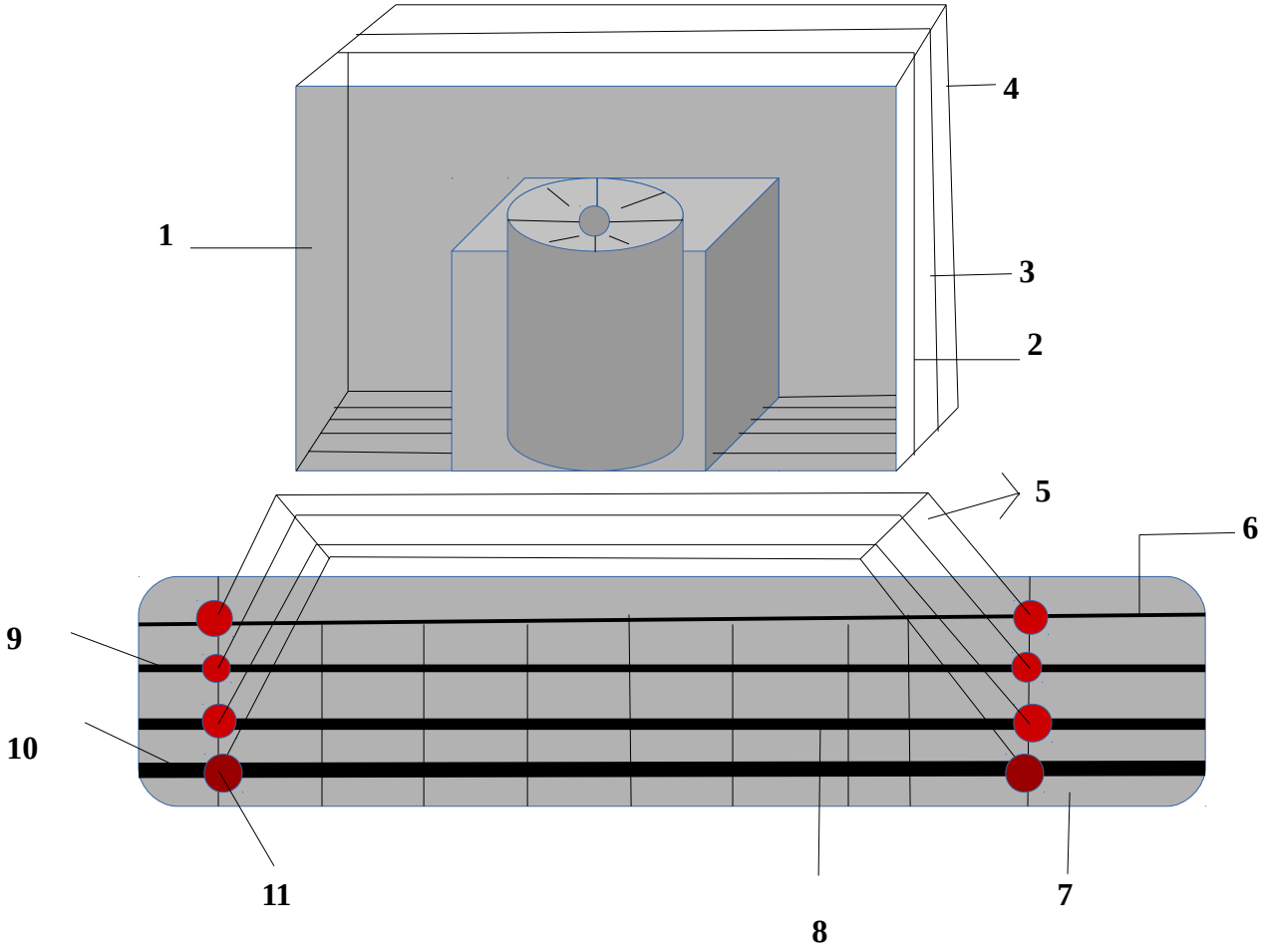
1). Fitting to hold Memory Chips
2). Banks 2 banks per memory chip 256 per bank total 512 bit addressing scheme
3). Data Strings 2 strings per Bank 128 bits per string total 4 strings per chip 512 bit addressing
4). Area Memory Bridge (Bytes to Frames switches)
5). 4 data strings per bridge 128 bits per wire total 512 bits
6). Reserved Memory area (Buffer) 1024 bits
7). Fiber Optic tube address encasement
8). Address Bridge 4 wires 128 bits per wire to process Fiber Optic

Model Super Sonic 75 Motherboard- Design Rev 1.3 3-A General View



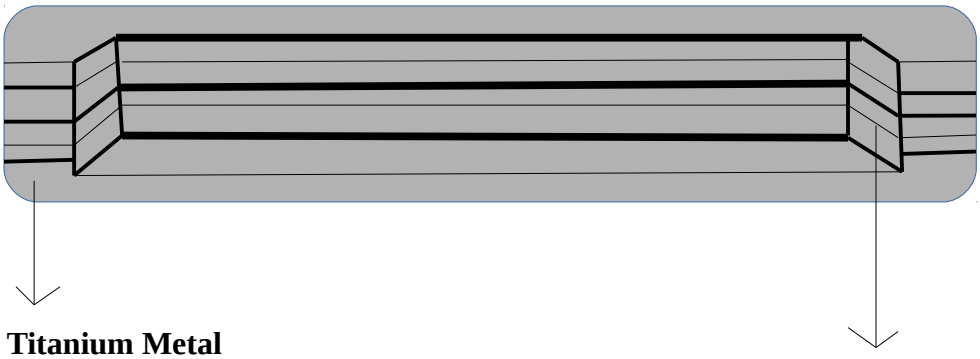
1). Public CPU Area of Space 4096 Bits
2). Private CPU Area of Space 4096 Bits
3). Shared CPU Area of Space 4096
4). Reserved CPU Area of Space 3072 Bits
5). Fiber Optic Net
6). CPU Fitting

Model Super Sonic 75 Motherboard- Design Rev 1.3 4-A General View



1). Public Video Area Space
2). Private Video Area Space
3). Shared Video Area Space
4). Reserved Video Area Space
5). Video Data Bride 4 slots
6). Public Data String
7). Titanium video fitting
8). Shared Data String
9). Private Data String
10). Reserved Data String
11). Node Points (End to End point connection)

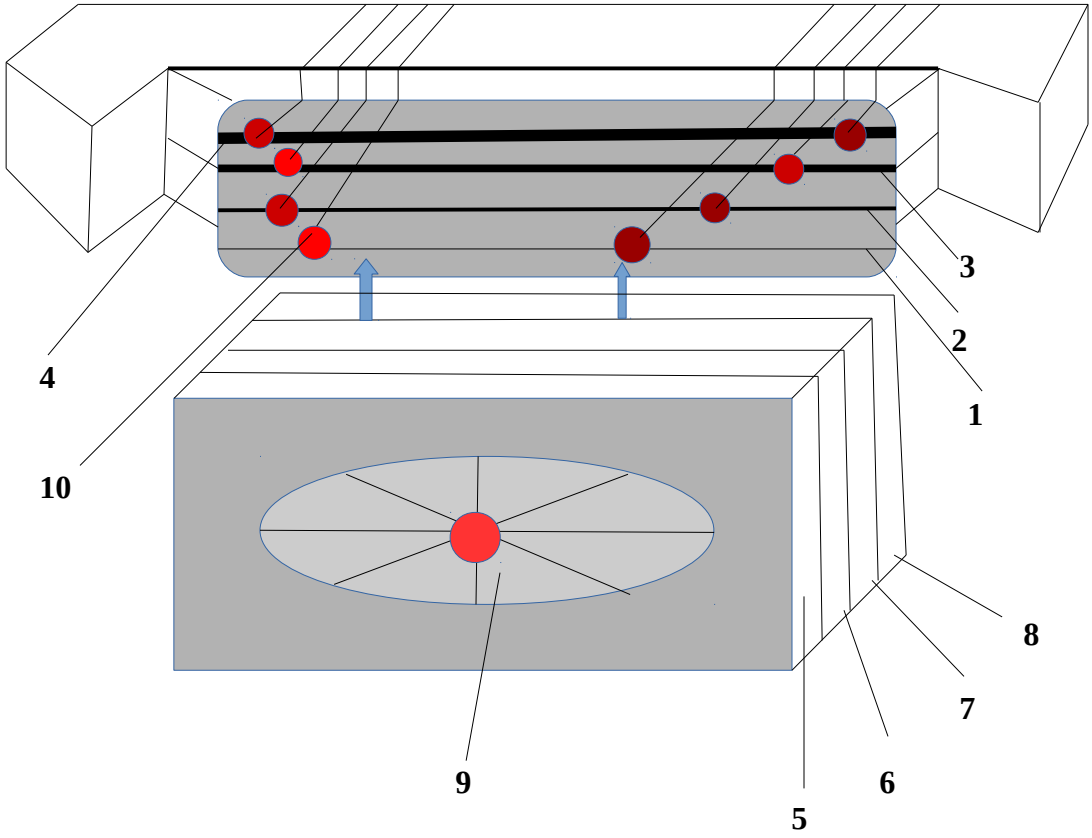
Model Super Sonic 75 Motherboard- Design Rev 1.3 5-A General View



Titanium Metal

Video Card Slot

Model Super Sonic 75 Motherboard- Design Rev 1.3 6-A General View



1	**Public Data String 128 bits**
2	**Private Data String 128 bits**
3	**Shared Data String 128 bits**
4	**Reserved Data String 128 Bits**
5	**Public Video Slot**
6	**Private Video Slot**
7	**Shared Video Slot**
8	**Reserved Video Slot**
9	**Video Fan**
10	**Node Points**

Overview of Design

I will be going over each component of the SS 75 Motherboard Design Version 1.3. Chart 1-A provides an overall view of the Model Design. The improvements I made took previous designs of the Models SS 65/75 with the following:

Chart 1-A

1). Major Components CPU, Memory Sticks, Video Slots now have four areas of space defined
   a). Public
   b). Private
   c). Shared
   d). Reserved

2). Each major Component of the motherboard now has 4 wires providing an internal network that allows for better interface and communication between components.

3). Other components sound adapters, Network adapters, External Connectors use a double ring as the new symbol so that Internal and External Devices within the Motherboard itself can be defined in later updated versions with Internal and External Energy to be defined as Asymmetrical.

4). The memory chips now have a External Reserved memory chip within the Memory space to allow for what we use to call buffer overflows basically a program can be qued and set in temporary storage until memory is freed up.

Chart 2-A

Chart 2-A is the component Memory and the improvements I made are the following:

1). Memory sticks now have 2 banks with 4 data strings that are 128 bits a piece for a total of 512 bits this allows for 512 bit addressing. In the past, the most for previous designs was 256 bits with no banks defined only Data strings. This allows for data string arrays to be defined in later versions.

2). As stated previously Memory now has an extra component and space defined as Reserved and is external this allows for temporary storage used as buffers to prevent overflows and bottlenecks.

3). Memory addresses are now defined as 512 bits and are encased in fiber optics to prevent questionable activities.

4). Data Brides are now employed on the Internal side of the Memory space areas to allow for better techniques for mac address assembly bytes to frames instead of a repeater physical switch.

Chart 3-A

Chart 3-A is the CPU this has been updated instead of three areas in previous designs there are now four with Areas of space defined updates include the following:

1). Areas Public, Private, and Shared utilize 4096 bits with 3 volts per space. The reserved area is defined as 3072 bits bringing the total number this CPU can handle is 15360 bits. The battery uses 12 volts meaning this design can handle up to 16384 bits but to allow for bit rotting and decay 1024 bits are reserved as a way to check for data integrity.

2). Node points are now limited or not being used because each node point represents a gateway to check weather it is on or off “1” on “0” off often creating a system bottleneck. The usage of fiber optic nets within the CPU still remain.

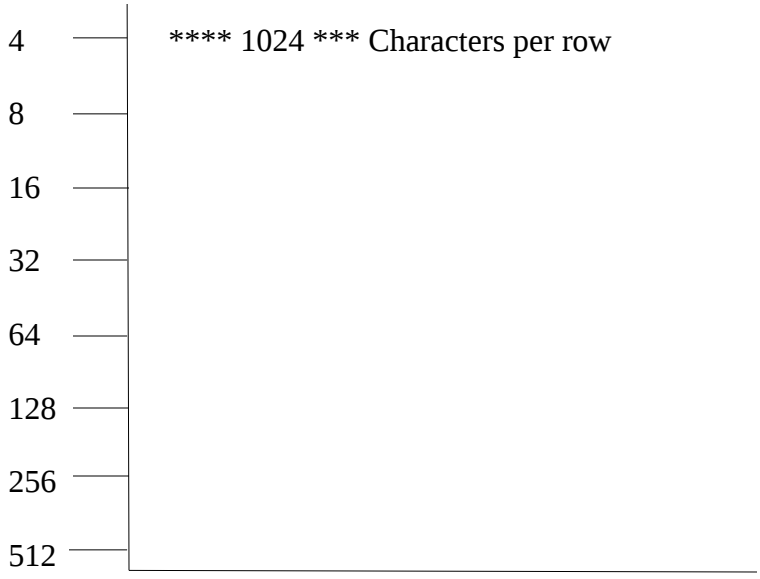
Chart 4-A

Chart 4-A is the video defined areas of space Public, Private, Shared and reserved. The video card has node points at each end point within the area of space similar to end to end point communications. Previous designs permitted data strings to constantly check the data string within the device which may create a bottleneck. The video slot also employs a data bride for byte to frame processing for each slot. The Data strings are defined as 128 bits for each space bringing the total to 512 bits.

Chapter 2

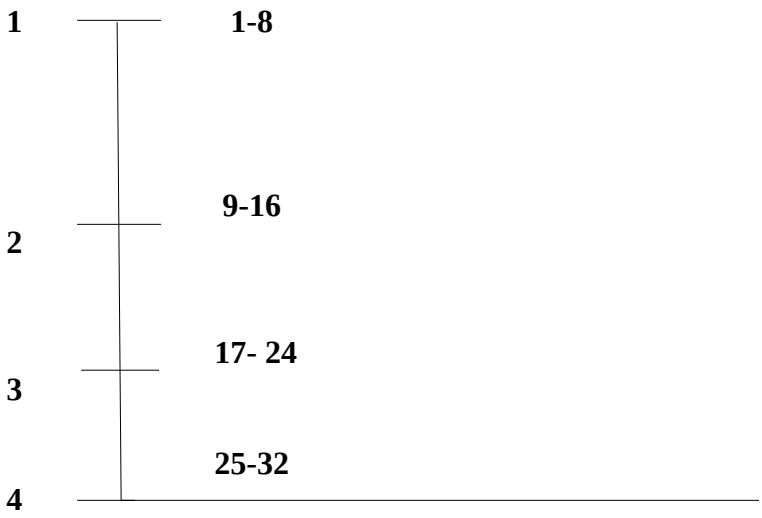
Single 8192 Data Block processing

I will begin by defining the block data of 8192 characters with the 512 bit addressing scheme from here I will create a matrix of 8 rows each with 1024 characters matrix. See chart below.



Since I have defined my address scheme as 512 bits. I divide 16384 bits = 8192 bytes by 512 bits and it comes up with 32 frames. I divide 32 frames by 8 to get the 4 packet of 2048 byte frames in bursts. To secure the data when sending outbound to the Internet or Intranet, I use a frame entanglement swapping frame 1 and 2. This is reassembled at the final destination or hop for old timers also this enforces endpoint to endpoint communication. I create four packets of 2048 byte frames equal to 8192 Characters. To create a even more secure environment, The user chooses which packets order is to be sent see chart below. I could even swap the last frame's of 31 and 32. The process is simple to follow take a 8192 block of data and create a matrix of 8 rows by 1024 characters this equals 8192 characters. The next step is to take 16384 bits divide by the address length 512 bits equals 32 frames swap frames one and two along with 31 and 32 next, create the IP Packet burst of 2048 with boundary's set for frame sequence processing and assembled at final destination. Client chooses which order is to be followed and assembles at final destination. A note on this I have recently in December 2017 created a 8192 byte file systems with password encryption on a external device so this can be achieved.

Packet # Frame sequence



4 packets of 2048bytes burst with frame sequences of 8.

Chapter 3

Group Frame to Packet Processing

Please remember the following OSI layer Stack Protocol Frame and Packet Processing

Physical	Bits to Bytes
Data Link layer	**Bytes to Frames**
a). MAC address Layer/Data Link Layer	**Bytes to Frames**
IP layer	Frames to Packets

The conversion and process is the following:

16384 Bits * 512 Bits = 8388608 bits / 1024 = 8192

The next step is to convert the bits into bytes this is dependent on how you represent characters in fields for example in the 80's you could use 2 bytes or 16 bits to represent 1 character in my presentation this equals 512 bits and I created an 8192 data block or 8 rows of 1024 Character blocks of Data.

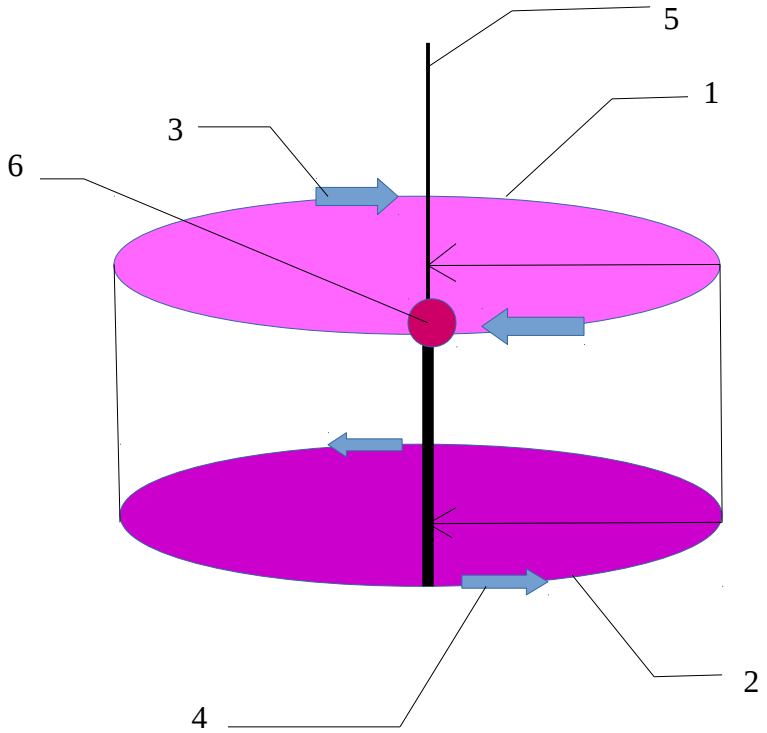
8388608 bits divided by 1024 = 8192 characters / 8 frames used for sequencing. This equals 2048 and than I select 4 because 2048 * 4 = 8192. The frames can be broken up because on the lower level second layer you create a sub-level within the second layer defining the mac address and how it is going to be used for frames into packets. This is a basic review. If you do not understand this, You may wish to study the OSI 7 layer stack and TCP/IP protocols.

I will now present my new cryptographic model in the next chapter.

Chapter 4

New Cryptographic Energy Model Design

Cryptographic Energy Model Visual Chart 1-B



1. Curvature Motion light Energy
2 Curvature Motion heavy energy
3. Clockwise motion
4. Counter Clockwise Energy Regeneration
5. Data String
6. Gateway Check node point

Cryptographic Energy Model Design

I will now present a New Cryptographic Energy Design based on Dynamic Heat and Asymmetrical Energy.

As you can see the energy in chart 1-B curvature is represented by darker shades of purple within the heat spectrum, When I regenerate into a darker color, I have more energy being regenerated.

Energy goes through a clockwise and counterclockwise motion. The Data sting when passing through to the heavier color uses a thicker line representing more energy with more allowance of bits. To check the Data String before going to the Darker shade of color goes through a Gateway check for Data Integrity.

This model uses a combination of both Linear and Curvature motion and Energy equating to a Cryptographic model design and will be employed in **next Generation patent Industrial Designs**.

Chapter 5

Final Thoughts

Final Thoughts

I have updated and have developed the SS 75 with the latest version 1.3 Motherboard Design known as Super Sonic. The updates include Video Slots with now four Area's of Space processing and 8192 Single and Group Character processing. I have created One video card slot with 4 Areas of space, Public, Private, Shared, Reserved Areas of space including now a data bridge at the data link layer with 128 bit data strings total 512 bits. These Strings use Fiber Optic Nets and Titanium. I have also updated the motherboard to include four wires that interface with the major components of the motherboard itself.

I have updated memory with the following specs 1 memory stick = two banks with each bank using two data strings for total or 512 bits for the addressing with future array processing.

The CPU uses 15360 bits with four areas of space with a reserved area of 1024 to prevent bit rotting and decay promoting data integrity this brings the total bits to 16384.

I have previously written and created a cohesive work that enforces the ideas I have attempted to convey in the past along in addition to some new concepts and or ideas that uses data node Points and strings. The node points uses uneven symmetry as far as size and spacing are concerned and limited to avoid system bottlenecks. The Data strings 128 bits use end node points that will be used for data integrity and checking.

I have limited the usage of node points to avoid system bottlenecks with less gateway processing checks of switches on and off.

I have taken a previous design and created a work that presents some new ideas worthy of consideration. I wish to thank you for taking the time in reading this work. In this work.

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02/15/2018

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Thank you for reading this work.