Introduction

Model SS17M-D

Model Super Sonic 17 Motherboard- Design and 15360 Bit Architecture

By

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Today is 07/15/2011 University Place, Washington. I would like to thank you for taking the time reading this scientific work. I have attempted to build upon the 12228 bit architecture and motherboard design by making and improving the design and employing some of the previous U.S. Copyrights registered for the purpose of taking theory's I have written and creating practical application to new theory's.

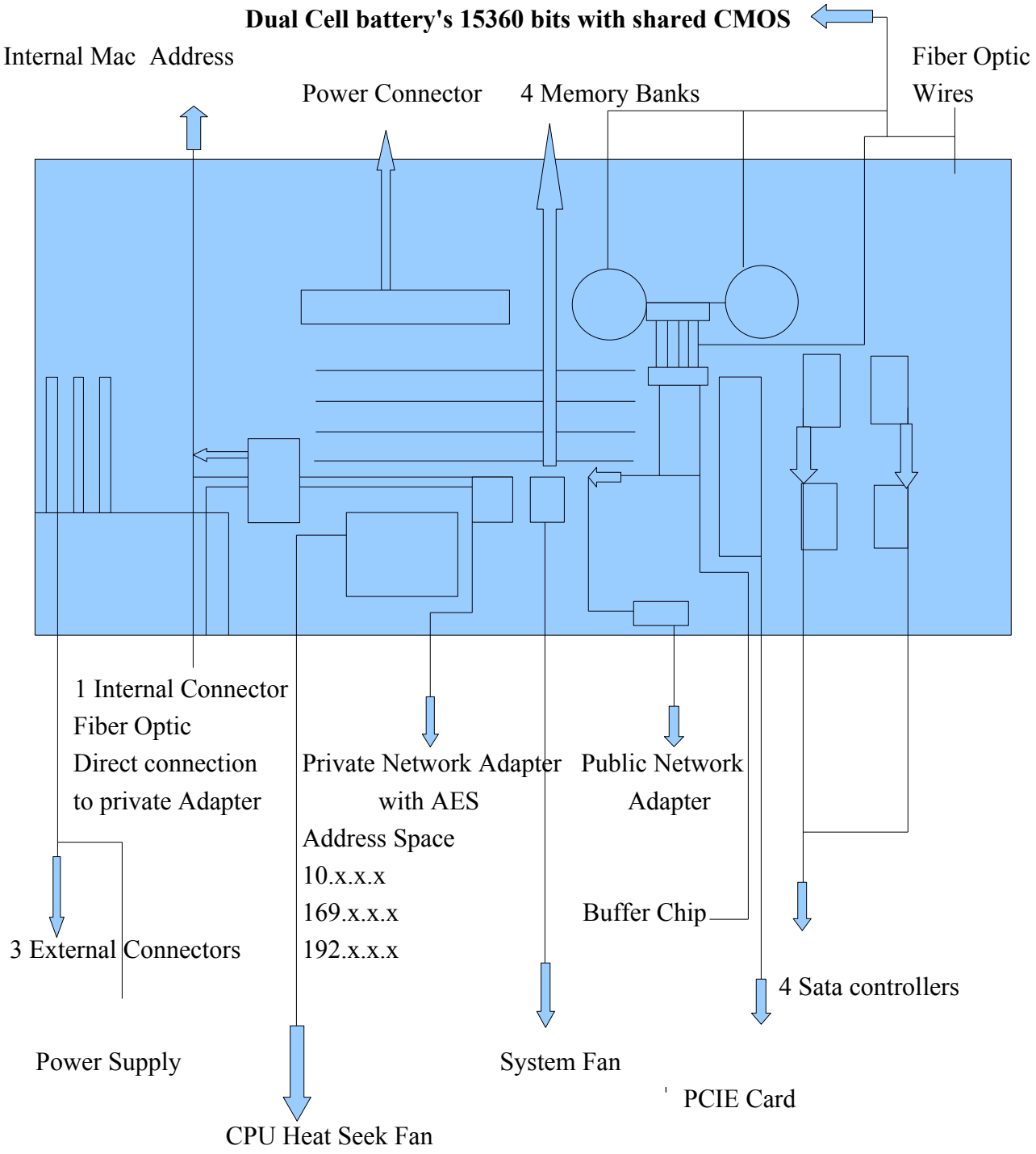
The Theory's I have written in my previous copyrights needed a answer as to how can a theory be made useful in everyday lives. Complex Theory, Design, and development is much like a ladder it takes gradual steps to arrive at a solution. I hope that if you have read my previous works you will find that in this paper some of the previous works being demonstrated such as Thoughts on Rotating Black Holes, OSI theoretical discussion, Visual Arts Equations, Temporal Spatial Equations and other works as a example. I want to take the time to thank you once again for reading and studying this paper.

The New Design feature's include the following improvements

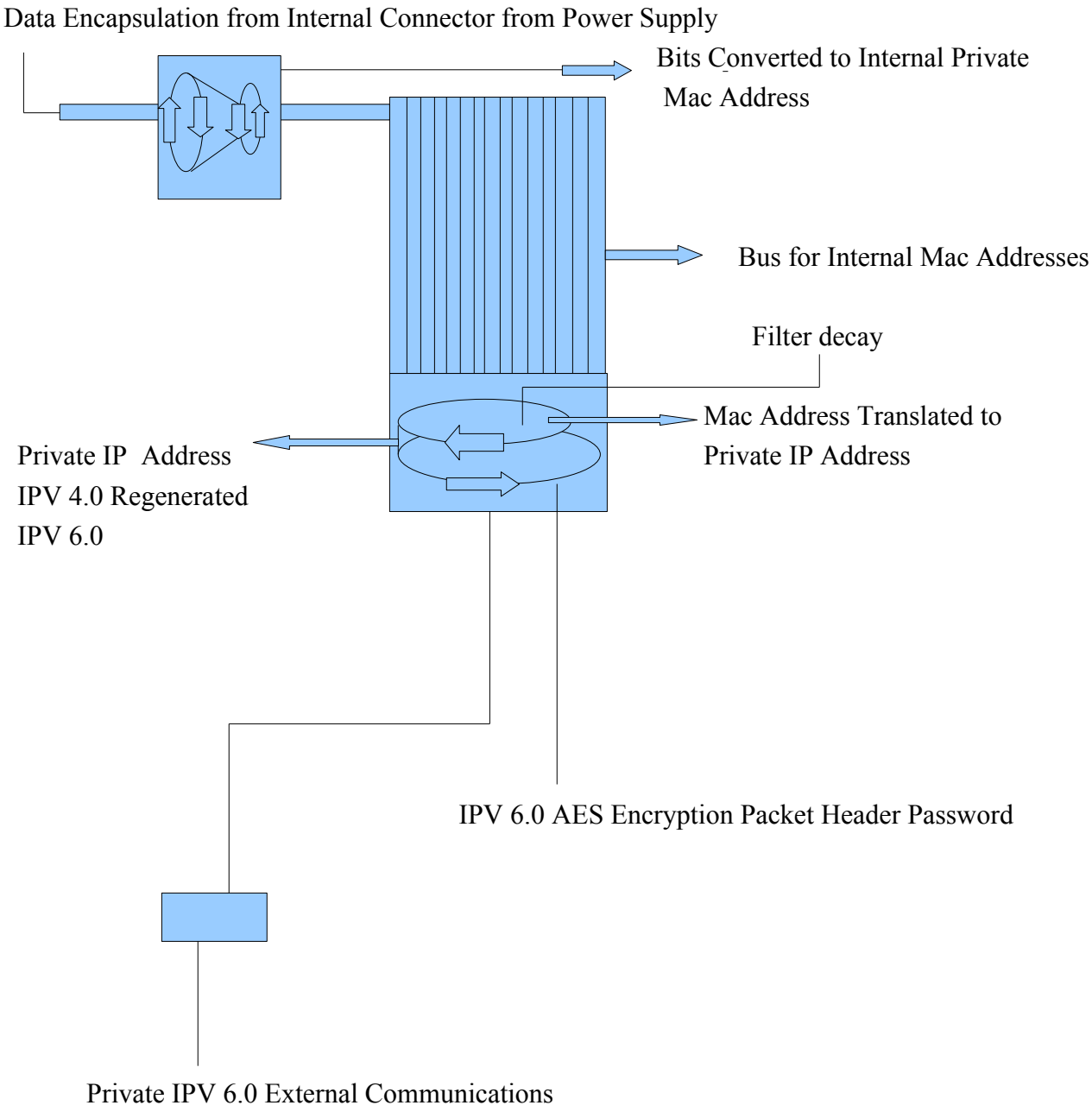
1). Power Connectors 3 External Connector's 1 Fiber Optic Internal Connector
2). Power Supply
3). BUS for Internal and External MAC address
4). Data packet delivery

Model SS17M-D

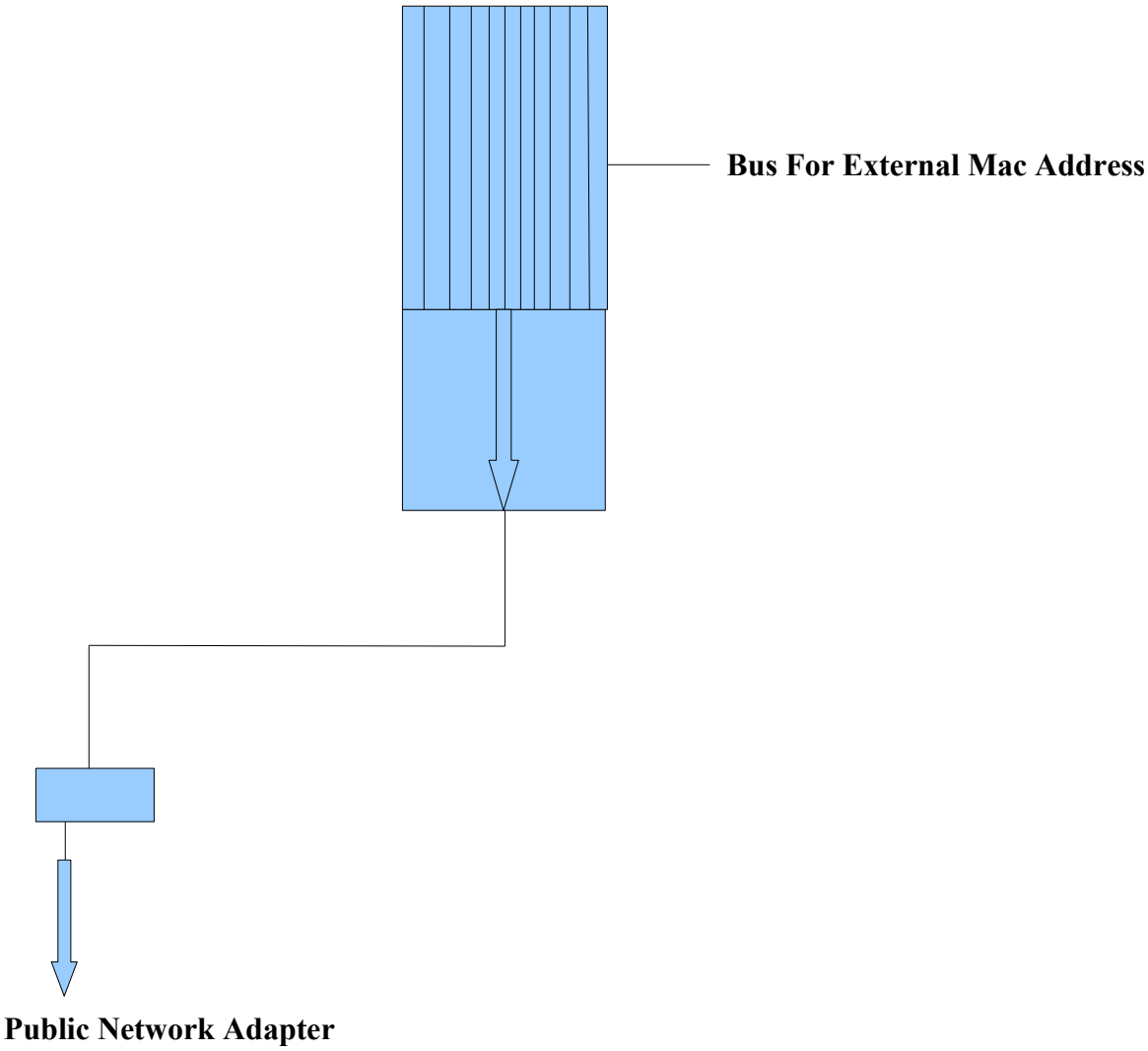
Model Super Sonic 17 Motherboard- Design



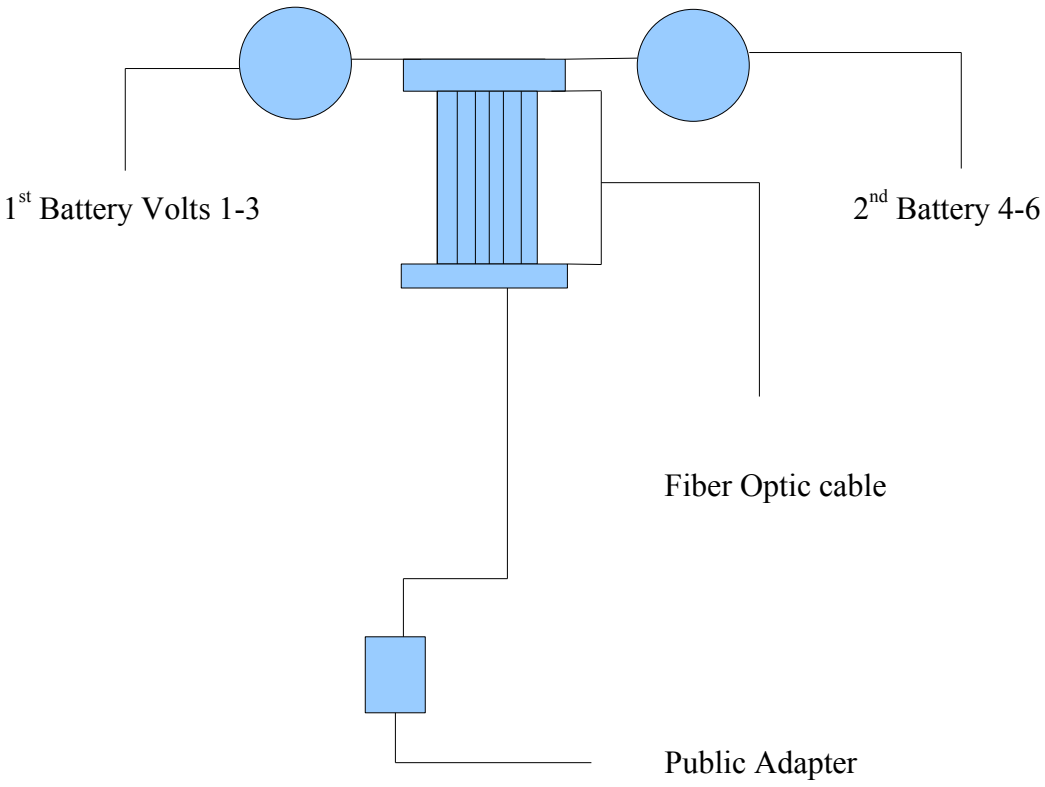
Internal Private Switch



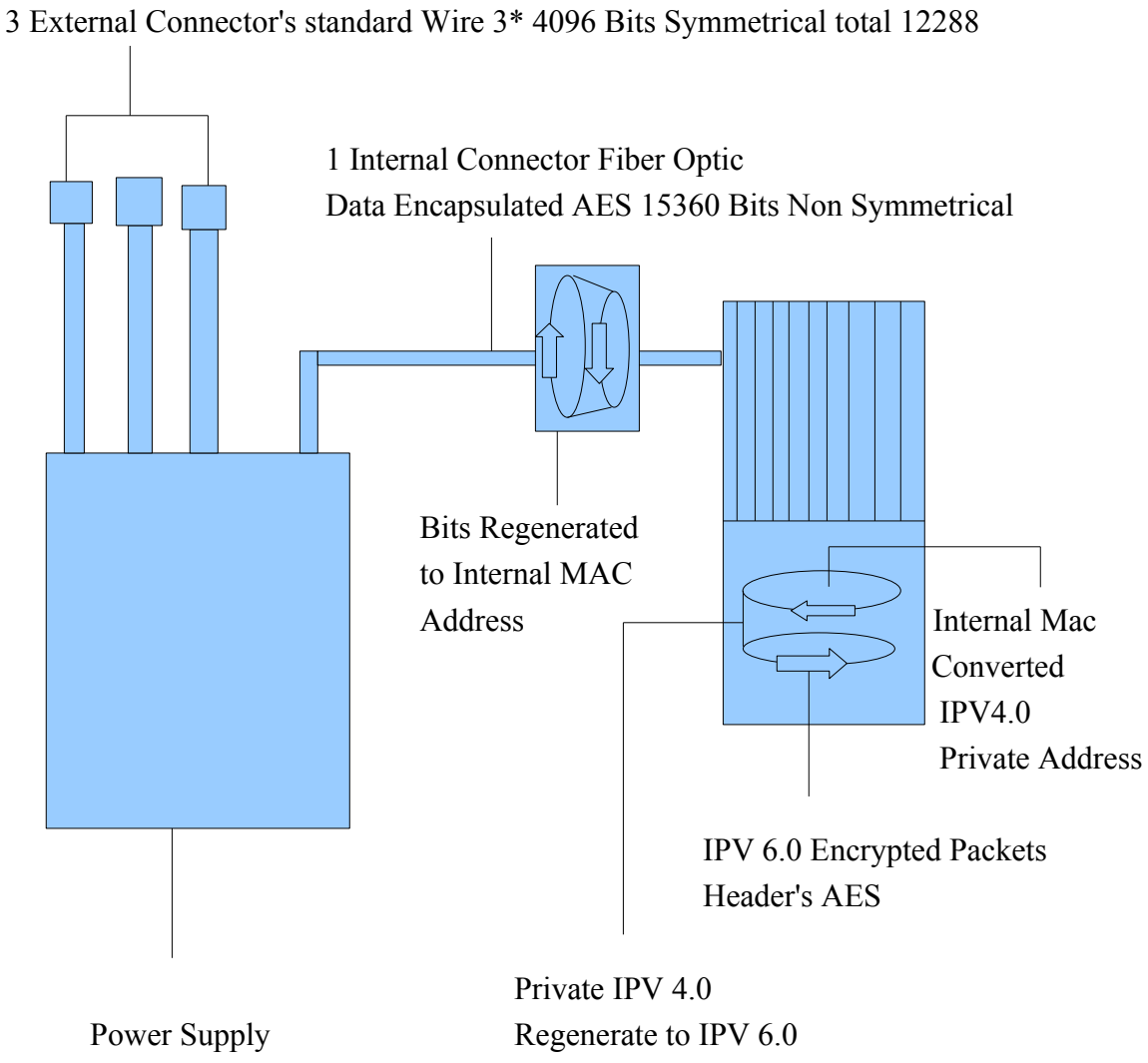
Internal Public Switch IPV 4.0



Dual Cell battery's 15360 bits with shared External CMOS



Power Supply



Internal Voltage to Bit Conversion Notes

The Power Supply has a Fiber Optic Cable that has Data Encapsulation thus it prevents less bit decay than it goes through a Rotating Black hole taking charged particles and Regenerating from Bits to a Internal Mac Address. In previous works Temporal Spatial Equations I proposed having data encapsulated to promote energy efficiency and effectiveness this allows bits from being exposed to External Environments that corrupt data for whatever reasons. The Internal Private Address allows for better usage of bits and I am able to deliver 15360 bits in a efficient manner compared to the External Power connectors utilizing 4096 bits per connector. The Private Internal switch allows time and motion to accelerate by saving wasted motion in the form of Packet delivery. A simple question would be which would be a better usage of energy 3 external connectors utilizing 4096 bits each for a total of 12228 or a Internal Data Encapsulated connector that utilizes 1 private switch at 15360 bits ? The obvious answer is the Internal Connector Data Encapsulated.

On another note, I attempted to keep the External Environment power connector's, Shared CMOS, Network adapter's from the the Internal Environment namely Data delivery, Network Adapters, MAC addresses separate because the External Environment allows for Energy to degradate at a faster rate than a Internal Environment thus by sharing resources it would cause a serious loss of Energy and Efficiency. Please note the External Power connectors each deliver symmetrical bits 4096 while the Internal Connector delivers uses a 4096 bits with 3 sub-keys that are not symmetrical.

External Power Connector's Voltage to Bits Chart

1st Battery Voltage/Bits produced

1st Volt	1024
2nd Volt	2048
3rd Volt	4096

2nd Battery Voltage/Bits Produced

4th Volt	8192
5th Volt	12288

6th Volt Reserved for Reallocation and Distribution

This is a conversion chart to show how many volts are to be converted from volts to bits. In my OSI Theoretical discussion I proposed a sub Physical layer at the lower stack of the OSI Please view the following

Network Layer frames assembled to packets IP Routing begins here
Data Link Layer Bytes into Frames Bridging begins here Non- Rout able
Physical Layer Bits into Bytes
Sub-Physical Voltage into Bits
Atomic Sub Particle layer Electrons, Proton Nucleus

Summary of New Features to 15360 Bit encryption

Today is 07/16/2011 University Place, Washington. I would like to go over my new board design with the new features that builds upon the 12228 Motherboard design and Architecture.

After reviewing the design diagrams, You will notice that I have added new design features in my 12228 bit motherboard design and architecture. Some of the new features are the following

1. External CMOS utilizes Public MAC and IP addresses no longer share Private Mac and IP addresses Data in the Internal Environment is protected.

2). The Power Supply utilizes 3 External Connector's each producing 4096 bits for a total of 12228 and 1 Internal Connector for 15360 Bits Data Encapsulated with Fiber Optic cable.

3). The Internal Power Connector Encapsulates bits that Regenerates them into Internal Mac Addresses and than is converted into IPV 4.0 Private IP addresses and is regenerated into IPV 6.0 addresses

4).The Private adapter allows IP headers to become encrypted using AES methods that are Non Symmetrical because the beginning process protects it from External Environmental pollution of Data Packets and Delivery along with signaling Interference

5). The Internal and External Network Switch's no longer share resources through CMOS when dealing with Data Delivery and signaling

6). The Public Network switch allows for Public IP addresses to be processed in regular fashion.

I have provided a brief summary and now I would like to go into greater detail about the new design which is entitled SS17M-D Motherboard design meaning Super Sonic 17 Motherboard Design which is the 3rd development to enhance privacy and security of End User Clients.

The 1st Design Feature Separates Internal and External Network Environments whereas the 3 power supply connectors are External and exposed to outside Environmental conditions. The Internal connector is not exposed to the outside but is Encapsulated using Fiber Optic cable and there is less waste of time and motion producing 15360 bits for the Internal connector .

The 2nd design Feature allows for the Internal Bits to go through a Regeneration process similar to a Rotating Black Hole it than produces Internal Mac addresses and is Data Encapsulated with Bit filtering at the 1st event the 2nd event produces Internal Mac Addresses and goes through a Fiber Optic cable and to the Private Network Adapter here it produces Private IPV4.0 addresses and than is Regenerated into IPV6.0 for External Environmental communications

The Private Network Adapter Encrypts Data packets in Non Symmetrical fashion thus it shows Dynamic usage of Energy making it non predictable in the case of time and motion because the 3 sub keys are Non Symmetrical. The Data Packets utilize AES Encryption with Header password security to prevent Data Piracy due to DNS Redirects by Public Server's and their administrator's.

I have attempted to provide a description of the new features and modifications of my previous design. I have chosen not to update the bus with Fiber Optic cables at this time because a determination of how may bits can be pushed through the bus will have to be reviewed carefully.

Testing and Experimental Notes

The following was tested from a software standpoint and showed very little problems.

1. Certificate of Authority E-mail Certificate 4096 Bits with 3 sub key encryption 1st sub key 4096 2nd sub key 4096 and 3rd sub key 3072 total bits 15360 bits creation of the certificate and sub keys tested okay and was able to send email and encryption to my trusted user which is my wife's E-mail account. The key was published. I produced another Certificate using the following parameters 1 Digital Signature 4096 2 sub keys 4096 total 8192 bits 1 sub key 2048 bits for a total of 14336 bits

2). Using Key Rings was able to implement MD-5 IP Packet Header Protection problem here is the uncooperative attitude when dealing with Data Centers and privacy. This is at best a 50 percent chance of success. When it is utilized this becomes a effective tool in sending secured E-mail and trusted web site information and validation.

3). I tested Ipv4 with link local Ipv6 limited in scope this worked okay especially when setting the firewall to TCP Reliable packets. I could not obtain automatic addresses when tested

4). SSH I created a RSA 8205 bit secure shell. This worked 1 time but was not tested again because of the Data Centers to let End User clients exercise the right to privacy also when checking Email client accounts for Authentication the one they allowed was Clear text or Login which

means a IP packet can be Re-directed and corrupted which is kind of baffling to not secure End-User Clients IP packets and allow for these kind of actions to continue. A Possible work around

5). I attempted to avoid applications that insist on total control dealing with file and property rights and choosing applications that will allow MD-5 or AES Authentication methods to be utilized.

6). This would mean applications that have a automation process will show to be ineffective while applications that require customization will fare better.

In conclusion, I have attempted to build upon my 12228 bit IT Architecture and Motherboard design by utilizing Internal Network switches which allows for Intelligent choice as to whether to utilize a Private or Public network switch thereby allowing bits to either Regenerate or decay which I first proposed in my previous U.S. Copyrights. I have attempted to Encapsulate Data which should allow for energy to be better harnessed and better utilized than to incur more loss of energy. The Fiber optic cable going from the power supply promotes Energy Efficiency and Effectiveness and allows for bits to be processed in a Internal Environment protecting it from External Environmental conditions such as Public address spaces that contain Virus attachments and other questionable activity. The upgrades as proposed is a gradual improvement of existing IT design, Architecture, and or implementation and should not be that hard for Computer Motherboard designers to implement on a industrial scale or commonly called Economy of scales.

The objective accomplished was to provide practical application to the previous U.S. Copyrights written because I believe it is not enough to write a theory and not provide a useful application to the theory proposed some examples are thoughts on Rotating Black holes, OSI theoretical discussion, Linear Cryptographic in Real time mode, Temporal Spatial Equations and Dynamic usage of Energy.

The Next Design Features will promote BIOS chips and Dynamic usage of External Devices not Encapsulated such as Hard Drives and memory Chips

Disclaimer because this work deals with Encryption and Data Security National Security Guidelines will be implemented in accordance with National law meaning Authorization to view this work will be strictly monitored.

Dated 07/17/2011

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