

**Model SS34M-D**

**Model Super Sonic 34 Motherboard- Design**

**By**

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## **Introduction**

Today is 08/29/2011 University Place, Washington. I would like to thank you for taking the time reading this scientific work. I have attempted to build upon the SS24M-D motherboard design by making and improving the design and employing some of the previous U.S. Copyrights registered for the purpose of taking theory's I have written and creating practical visual application to new theory's.

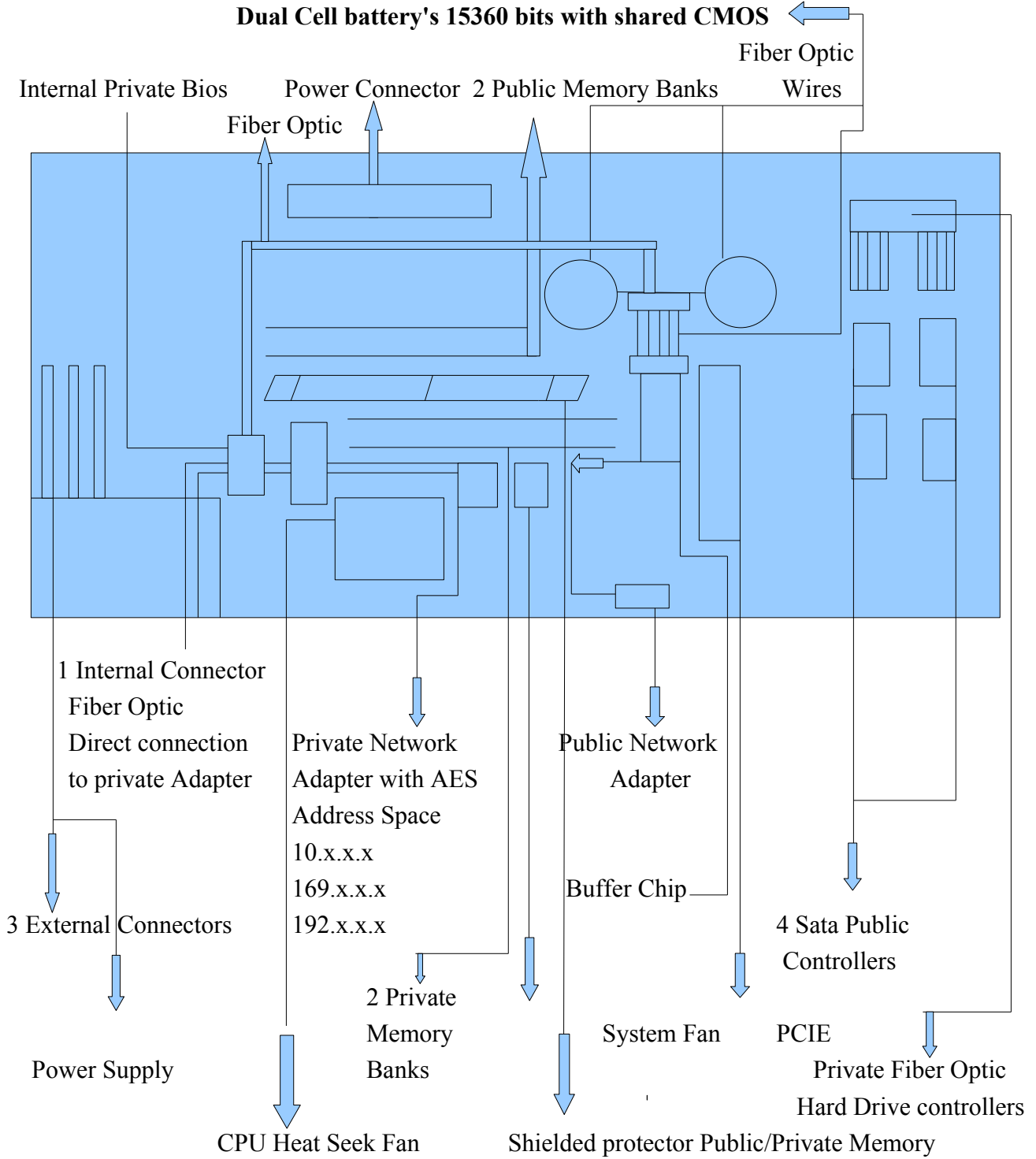
The Theory's I have written in my previous copyrights needed a answer as to how can a theory be made useful in everyday lives. Complex Theory, Design, and development is much like a ladder it takes gradual steps to arrive at a solution. I hope that if you have read my previous works you will find that in this paper some of the previous works being demonstrated such as Thoughts on Rotating Black Holes, OSI theoretical discussion, Visual Arts Equations, Temporal Spatial Equations, Why the Big Bang Theory is a Myth and other works as a example that answers the question above. I want to take the time to thank you once again for reading and studying this paper.

### **The New Design feature's include the following improvements**

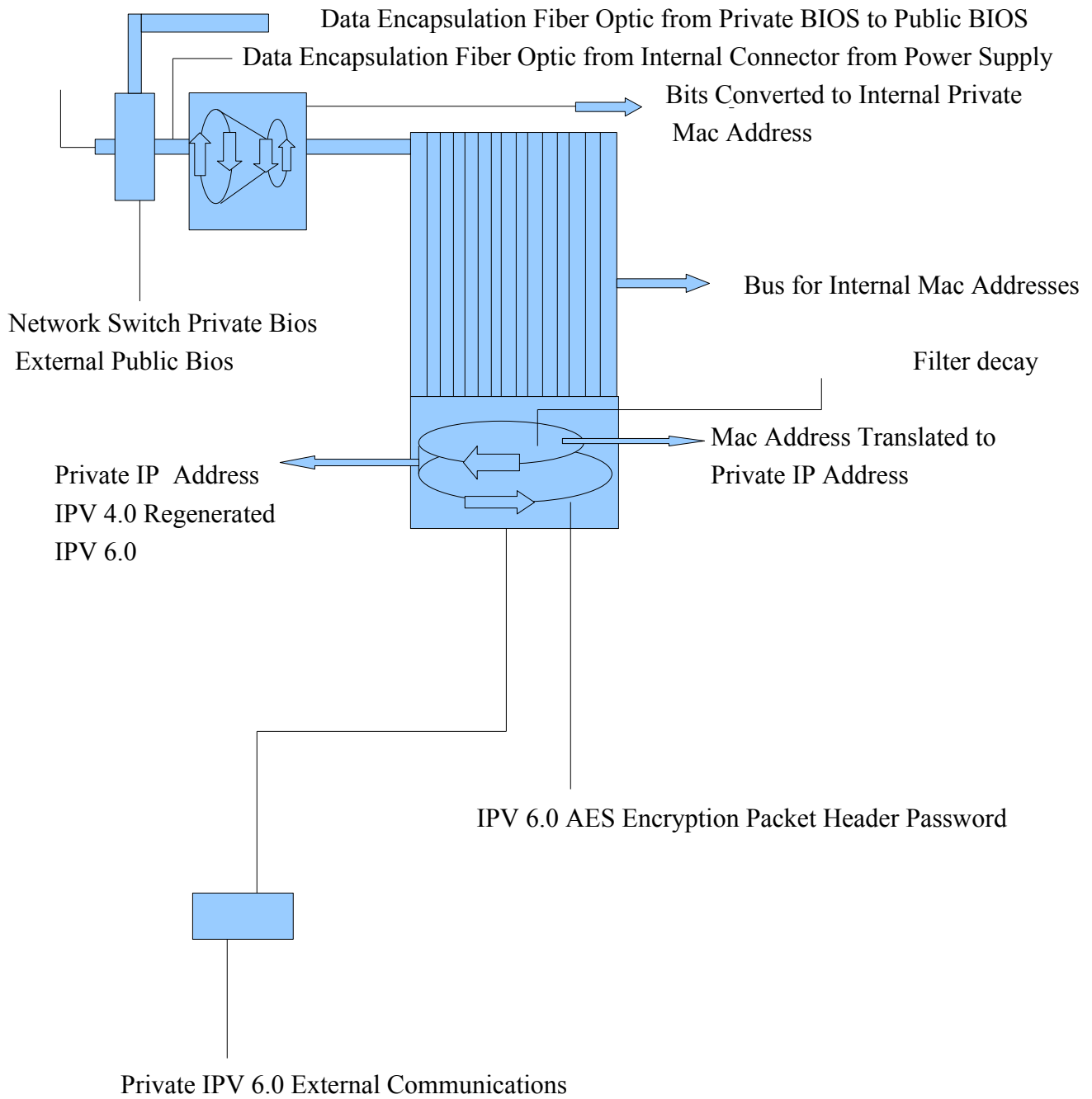
- 1). Public Sata Controllers
- 2). Private Non Symmetrical Fiber Optic Hard Drive Controller's
- 3). Public Memory Banks Symmetrical Application Access
- 4). Private Memory Banks Non Symmetrical Application Process
- 5). Shielded Protector prevent Interference from Cross talk/Noise/Interference

# Model SS34 M-D

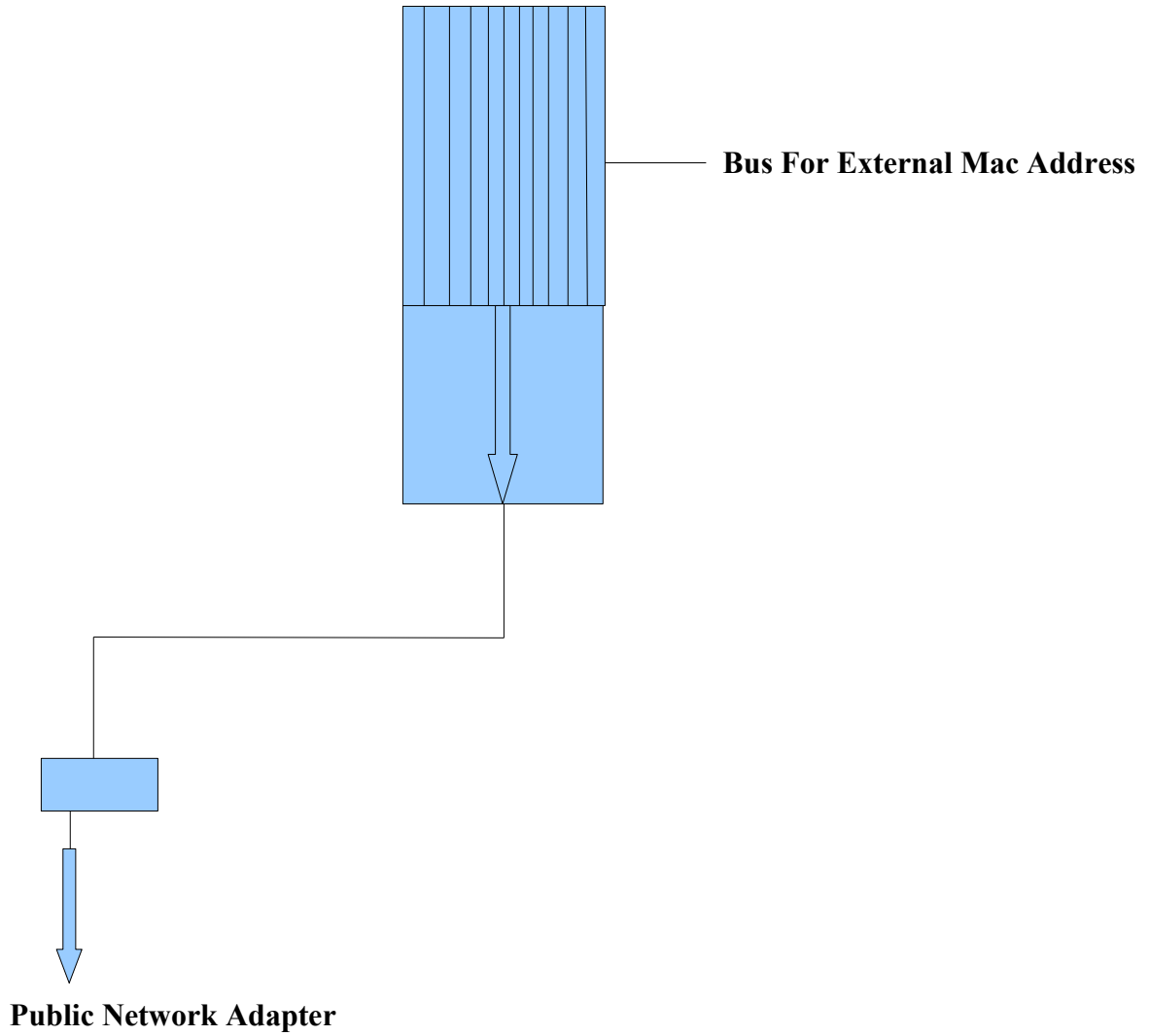
## Model Super Sonic 34 Motherboard- Design



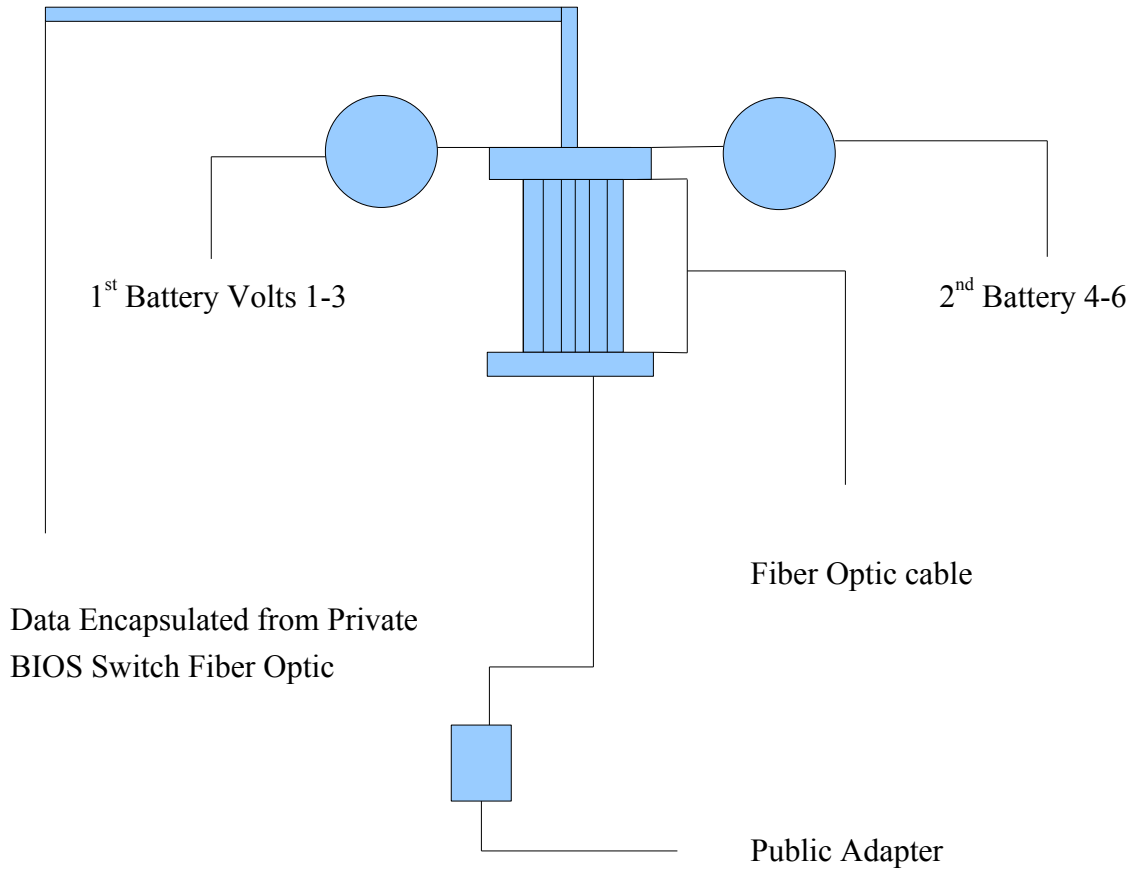
## Internal Private Switch



### Internal Public Switch IPV 4.0

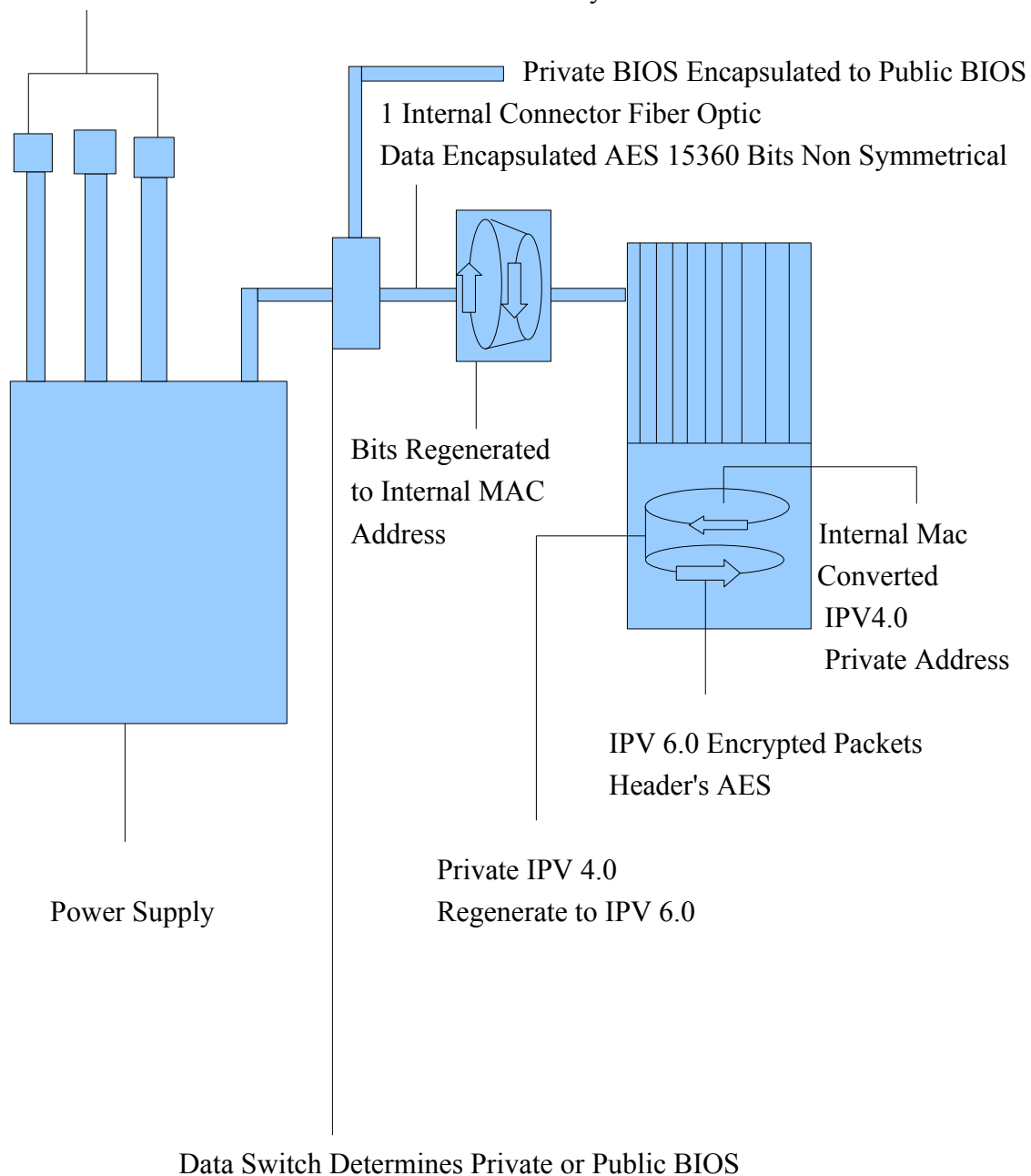


### Dual Cell battery's 15360 bits with shared External CMOS

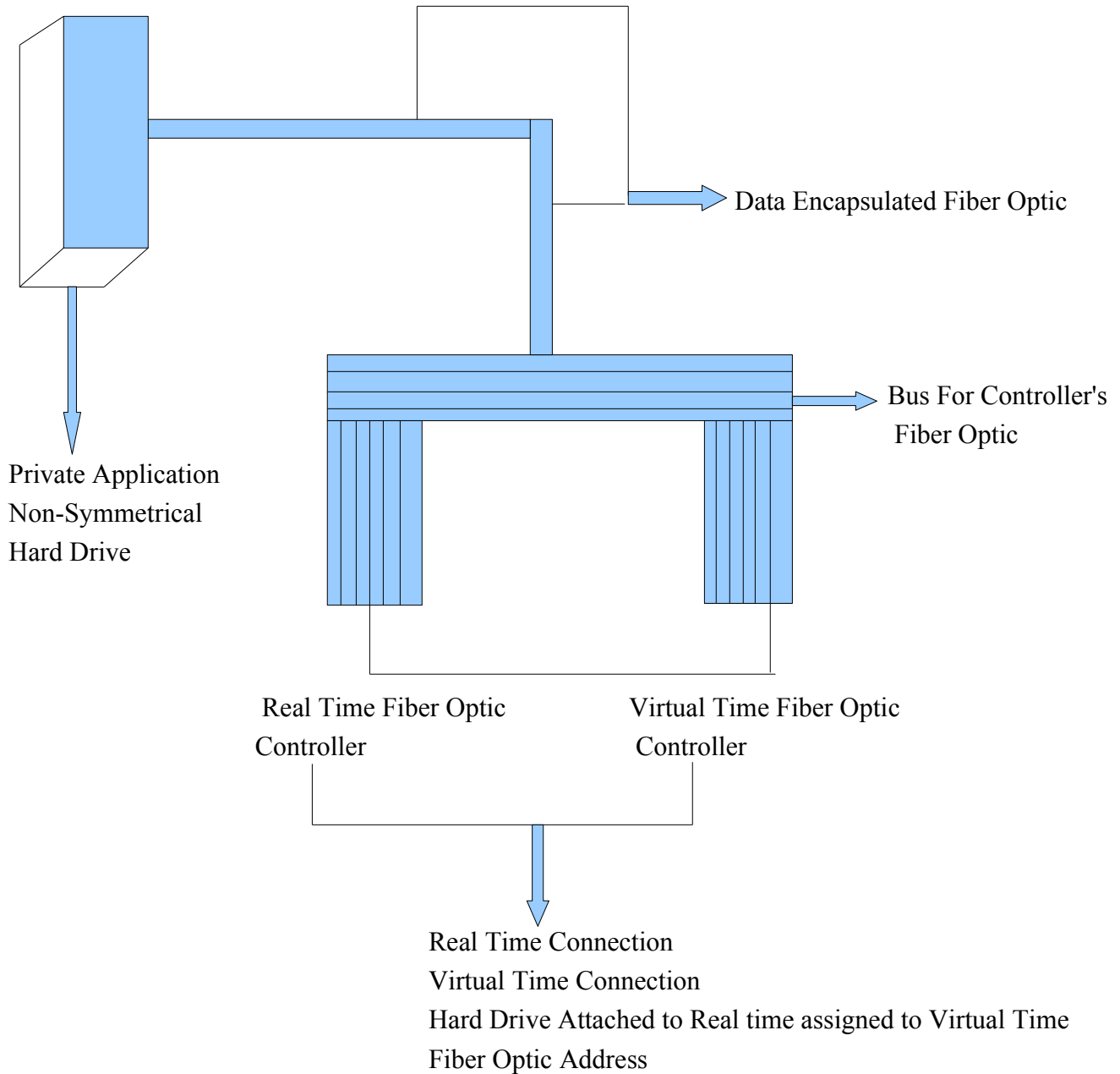


## Power Supply

3 External Connector's standard Wire 3\* 4096 Bits Symmetrical total 12288

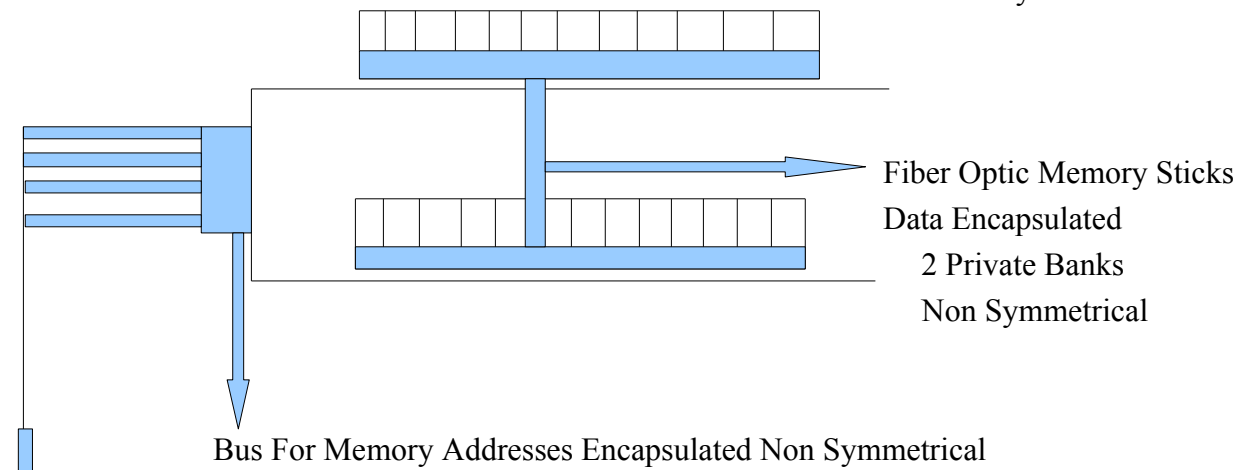
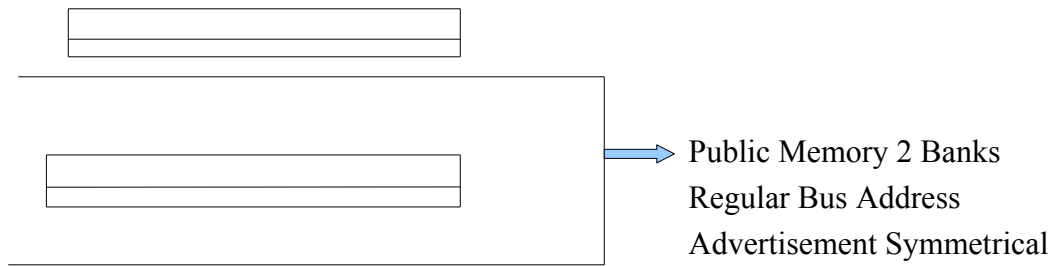


## Private Hard Drive and Non Symmetrical Fiber Optic Controller's





### Private Non Symmetrical and Public Symmetrical Memory



Bus For Memory Addresses Encapsulated Non Symmetrical

Memory Addresses Data Encapsulated Fiber Optic

## **Processing Features of SS34M-D Design**

The Power Supply has a Fiber Optic Cable that employs Data Encapsulation thus it prevents less bit decay and promotes data security in a Internal Environment. The next step is it goes to a Data Switch requesting either a Private or a Public Bios. If it goes to the Public Bios the Data is encapsulated via Fiber Optic to prevent external environmental corruption it then proceeds with normal symmetrical processing which is Public Address spaces. If it goes to the private Bios, Than it goes through a Rotating Black hole taking charged particles volts and Regenerating from Bits to a Internal Mac Address . Addresses are loaded from Private Memory Banks that are Non-Symmetrical and Applications are accessed from a Private Hard-Drive that is also Data Encapsulated. This is critical because Network Security involves managing objects, file's and Property rights by defining what is Private and Public this will enhance IT security by keeping Public Applications, file's and objects non-accessible to Private Administration by defining the processes as symmetrical and Non Symmetrical

In previous works, I have basically shown When Hardware and Software from a System standpoint is to be loaded with Security and Privacy feature's. I am now attempting to create a Dynamic environment by showing Network Administration to be Dynamic by creating instant creation of Environments by Intelligent design either Public or Private. A question maybe asked as to how Private Applications can be used and placed on a private Hard Drive ? One solution is to define Flash Drives as to whether they are Symmetrical or Non Symmetrical meaning if a Symmetrical Flash drive attempts to access a Private Hard drive it will not be permitted because it is programmed within a shell or Internal Environment as defined parameters of that device and within the Bios.

## External Power Connector's Voltage to Bits Chart

### 1<sup>st</sup> Battery Voltage/Bits produced

1 <sup>st</sup> Volt	1024
2 <sup>nd</sup> Volt	2048
3 <sup>rd</sup> Volt	4096

### 2<sup>nd</sup> Battery Voltage/Bits Produced

4 <sup>th</sup> Volt	8192
5 <sup>th</sup> Volt	12288
6 <sup>th</sup> Volt	Reserved for Reallocation and Distribution

This is a conversion chart to show how many volts are to be converted from volts to bits. In my OSI Theoretical discussion I proposed a sub Physical layer at the lower stack of the OSI Please view the following

Network Layer frames assembled to packets IP Routing begins here  
Data Link Layer Bytes into Frames Bridging begins here Non- Rout able  
Physical Layer Bits into Bytes  
Sub-Physical Voltage into Bits  
Atomic Sub Particle layer Electrons, Proton Nucleus

## **Summary of New Features of SS34M-D Motherboard Design**

Today is 08/29/2011 University Place, Washington. I would like to go over my new board design with the new features that builds upon the SS24M-D Motherboard design and Architecture.

After reviewing the design diagrams, You will notice that I have added new design features in my SS34M-D motherboard design and architecture. Some of the new features are the following

1. Separate Private and Public Memory Banks with a Protected Shield. Data Encapsulation within the Private Memory area of space via Fiber Optic
- 2). Private Hard drive Controller's to protect against Environmental pollution utilizes Dynamic Virtual Port Addresses. Public Hard Drives utilize Sata Controller's.
- 3). Private Hard drive that is Data Encapsulated from the Private Fiber Optic Controller
- 4). Network Administration is Defined by Private Non Symmetrical Processing utilizing Data Encapsulation verse Public Symmetrical processing in Non Data Encapsulated Format.

## **Details on New Features**

I have provided a brief summary and now I would like to go into greater detail about the new design which is entitled SS34M-D Motherboard design meaning Super Sonic 34 Motherboard Design which is the 4<sup>th</sup> development to enhance privacy and security along with Energy Efficiency

The 1<sup>st</sup> Design feature is Private Controller's that encapsulate data to the private Hard Drive utilizing Fiber Optics and Non Symmetrical Processing. The Private Controller's have 2 ports the 1<sup>st</sup> one is where the Private Hard Drive is actually attached this is called the Real Time Connection. The 2<sup>nd</sup> Port is where the Hard Drive addresses is located at a Virtual port which utilizes a Dynamic table of addresses. This is called a Inverse relationship. The address is already loaded before the event occurs' than the controller Real Time connection pulls the Virtual port address. This principle is similar to the Paper I written regarding Tachyon particles and dealing with sub-atomic particles..

The 2<sup>nd</sup> Design Feature has Separate Memory Banks Private and Public. The Private Memory banks are loaded after the Initial choice is Private Bios. The addresses are loaded in Non Symmetrical type processing in Dynamic mode with Data Encapsulation occurring at 2 points to prevent cross talk, Noise, and signal Interference. The 1<sup>st</sup> is the Private Memory Sticks have a fiber optic cable that is attached to one another to share resources within the Internal Environment. The next is when the addresses wish to advertise private services it is encapsulated via Fiber Optic to prevent addresses being exposed to Wireless Hacker's.

The 3<sup>rd</sup> Feature is a Shield or similar to a wall placed between the Public and Private memory banks to prevent addresses from being exposed to signal Interference.

The 4<sup>th</sup> Feature is Applications are defined by Private Non Symmetrical and Public Symmetrical so that in a Private Environment Files, objects' and Property rights undergo further evaluation also it prevents Public Network Administration to manipulate objects, files, and properties by defining it as either Symmetrical or Non Symmetrical. In a Private Administrative environment the Network Public Administration would not be given any access unless it agrees to Private Non Symmetrical Dynamic Environmental controls.

The 5<sup>th</sup> Feature is SATA Controller's are not defined as Public Address spaces meaning it will not have access to Private Encapsulated Data and the Dynamic Addresses. Today's motherboard designs allow for Public and Private Access which is a problem for Privacy and Security when trying to secure the User who paid for their PC.

## **Summary of design Considerations**

In conclusion, I have attempted to build upon my SS24M-D Motherboard design by separating and Encapsulating Private and Public Memory sticks and Hard Drives ;thereby, allowing Intelligent choice as to whether to utilize Private or Public Applications with the ability to define Network Administration as well. I have also created for Public spaces a Static Environment that is Symmetrical in nature vs Private Dynamic Environment that is Non Symmetrical with Data protected via Encapsulation to prevent Environmental corruption of Data to insure privacy and security.

I would like to build upon my previous Pseudo code that could be used for processing Public and Private Data and Applications.

## Pseudo Code for Processing Address Spaces

A = Private Bios

B = Public Bios

Default = Public Bios Default

If A

then

Goto Private BIOS processing

Else

If B

then

Goto Public Bios processing

Else

Goto Public Bios



## **Private Bios Processing**

Non Symmetrical Processing begins

Bits are filtered and decay begins at the 1<sup>st</sup> Event

Bits are processed into Bytes which are converted into Internal Mac addresses

MAC addresses are loaded into a table for Private Memory Storage Encapsulated

Private Hard Drive Pulls Memory Addresses to load Applications

Internal Mac address are converted into Private IPV 4.0 addresses

2<sup>nd</sup> Event Private IPV 4.0 are Regenerated into IPV 6.0 with Packet Encryption and Headers using AES

Packets ready for Private communications employing Privacy and Security

## **Public Bios processing**

Symmetrical processing begins

Data Encapsulated from Private BIOS via Fiber Optic

Public Mac Addresses are loaded into tables Public Memory Spaces

Public Hard Drive Pulls Memory Addresses for Applications

Public BIOS settings loaded using IPV 4.0 utilizing Public Switch.

End

This is a sample code and Instructions on how this can be implemented. The idea here is to take Private and Public Mac Addresses loaded them into a table as memory spaces for each Environment than they are accessed through the Hard Drive depending whether it is a Public or Private Hardware Device. Please find below the Screen for the initial Pre Boot-up procedure.

## **Initial Bios Boot Up Screen**

### **BIOS Consumer End-User Select Screen**

- 1). Select 1 For Private Bios For Privacy and Security
  
- 2). Select 2 for Public Bios For Social Networks

Default is Public Bios if 1 or 2 Not selected after 10 Seconds.

## **Conclusion and Summary**

The objective accomplished was to provide practical application to the previous U.S. Copyrights written because I believe it is not enough to write a theory and not provide a useful application to the theory proposed some examples are thoughts on Rotating Black holes, OSI theoretical discussion, Linear Cryptographic in Real time mode, Temporal Spatial Equations and Dynamic usage of Time and Space, and Why the Big Bang Theory is a Myth. If you are interested in other works that incorporate Physics, Mathematics, and Computers, Please visit my web site below.

Dated 08/29/2011

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